DETAILED ACTION

1.   Applicant's amendment filed on March 12, 2010 has been entered. Claims 1-20 are pending. Claims 4 and 15 are cancelled by the applicant.

Examiner's Amendment

2.   An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given by applicant on March 23, 2010. The applicant has agreed and authorized examiner to amend claims 1 and 13 to overcome the lack of antecedent basis in the above mentioned claims.

CLAIMS:

3.   <u>Please replace claim 1 as follows</u>:

Claim 1.   (Currently Amended) A method, comprising:

executing a software object;

establishing a security level for said software object, wherein the security level is directly related to said software object;

performing a multi-table input/output (I/O) space access using at least one of said security levels, wherein performing the multi-table I/O space access further comprises:

establishing a secondary I/O table;

receiving an I/O space access request based upon executing of said software object;

performing a multi-level table access based upon said I/O space access request using said secondary table and at least one virtual memory table; and

accessing at least a portion an I/O device based upon said multi-level table access; and

executing a function of said <u>software</u> object, wherein executing said function comprising accessing at least a portion of said input/output space.

4.   <u>Please replace claim 13 as follows</u>:

Claim 13.   (Currently Amended) An apparatus, comprising:

a processor coupled to a bus;

means for coupling at least one software object to said processor;

an input/output (I/O) device; and

an (I/O) access interface coupled to said bus and [[said]] a memory unit, said [[memory]] (I/O) access interface to provide said processor a multi-level table I/O space access of at least a portion of said memory unit based upon at least one security level, in response to said processor executing said software object, wherein the security level is directly related to said software object wherein said I/O space access interface comprises an I/O space access table coupled with a secondary I/O table, said memory access interface to provide a virtual memory addressing scheme to access at least one portion of said I/O device based upon a security level.

Information Disclosure Statement

5.   The information disclosure statement (IDS) filed on April 15, 2009 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

6.   Claims 1-3, 5-14, and 16-20 are allowed. The following is an examiner's statement of reasons for allowance:

The prior art does not disclose establishing a security level for said software object, wherein the security level is directly related to said software object; performing a multi-table input/output (I/O) space access using at least one of said security levels, wherein performing the multi-table I/O space access further comprises: establishing a secondary I/O table; receiving an I/O space access request based upon executing of said software object; performing a multi-level table access based upon said I/O space access request using said secondary table and at least one virtual memory table; and accessing at least a portion an I/O device based upon said multi-level table access, as set forth in claims 1 and 12.

The prior art also does not disclose establishing a security level for said software object; establishing a secondary input/output (I/O) table; receiving an I/O space access request based upon executing of said software object; determining at

least one security level that corresponds to a segment in said secondary I/O table; verifying a match between an execution security level to a security level associated with a segment being accessed in response to an execution of said software object; determining an I/O space address based upon said secondary I/O table in response to a match between said execution security level and said security level associated with said segment being accessed; locating a physical I/O device location corresponding to said I/O space address; and accessing a portion of an I/O device based upon locating said physical memory location, as set forth in claims 8 and 17.

The prior art also does not disclose an (I/O) access interface coupled to said bus and a memory unit, said (I/O) access interface to provide said processor a multi-level table I/O space access of at least a portion of said memory unit based upon at least one security level, in response to said processor executing said software object, wherein the security level is directly related to said software object wherein said I/O space access interface comprises an I/O space access table coupled with a secondary I/O table, said memory access interface to provide a virtual memory addressing scheme to access at least one portion of said I/O device based upon a security level, as set forth in claim 13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhnga (Tanya) Truong whose telephone number is 571-272-3858.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Taghi Arani can be reached on 571-272-3787. The central fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

/Thanhnga B. Truong/

Primary Examiner, Art Unit 2438

TBT

March 22, 2010